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[SYSTEM AND METHOD FOR ARBITRATION BETWEEN SHARED PERIPHERAL CORE DEVICES IN SYSTEM ON CHIP ARCHITECTURES]

Abstract

A system for implementing arbitration between one or more shared peripheral core devices in system on chip (SOC) integrated circuit architecture includes a first microprocessor in communication with a first system bus, and a second microprocessor in communication with a second system bus. At least one peripheral core device is accessible by both the first microprocessor and said second microprocessor, and an arbitration unit is in communication with the first system bus and the second system bus. The arbitration unit is configured to control communication between the at least one peripheral core device and the first and second microprocessors.